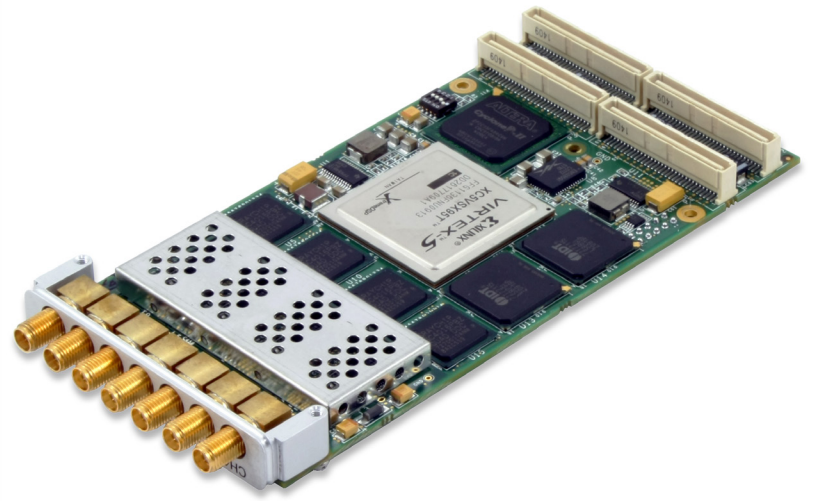


ICS-1555

4-Channel, 160/180 MHz 16-bit ADC PMC Module with Virtex-5 SX95T User Programmable FPGA

Designed for communications, radar and test & measurement applications, the ICS-1555 builds on the legacy of the industry-leading ICS-554 and ICS-1554 digital receiver family to provide unsurpassed ADC technology with industry-leading DSP expertise. The result is a cost-effective combination of size and performance in a single PMC site.

The ICS-1555 consists of four 16-bit ADCs sampling synchronously at frequencies up to 160 MHz or 180 MHz. Simultaneous down conversion of up to 16 arbitrary signal bands is provided by four Graychip GC4016 digital down-converters (DDCs). A Xilinx Virtex-5 SX95T FPGA is provided for user-defined signal processing functions, giving greater capacity and lower power consumption than previous generations.

The DDCs provide digital down-conversion of up to 16 narrowband, eight Split-I/Q or four wideband channels that can be tuned to any arbitrary center frequency within the pass band. Output data can be in either real or complex format, providing a maximum bandwidth of 10 MHz (-1dB) on each channel.

The sampling clock can be generated internally using the onboard Silicon Labs Si571, a modern Crystal Oscillator with programmable frequency and a stability of +20 ppm. The sampling clock can also be sourced externally by powering down the onboard oscillator and providing a clock input on the front panel connector. The external clock can be a sinewave or LVTTL signal with a frequency in the range of 32 MHz to 180 MHz.

The FPGA is not used for board control functions, thus providing maximum occupancy for customer applications. It provides a powerful signal processing capability that can be loaded with standard functions such as wideband DDC, FFT and time stamping, or programmed by the user for any required field.

The programmable clock can be referenced to an internal 10 MHz reference with a stability of ±1 ppm or referenced to an externally supplied clock in the range of 10 - 200 MHz.

The product provides internal and external clock and trigger capability, and supports multiple board synchronous sampling both of ADC and DDC functionality.

A Hardware Development Kit (HDK) provides support for users who wish to implement their own signal processing algorithms in the FPGA. Alternatively, our FPGA applications programming team can develop FPGA cores specific to customer needs. For more information on standard processing functions or custom development, contact your local sales manager.

64 User I/Os connected directly from the FPGA to the Pn4 connector provide an alternative high-speed data path to the module. The I/O pins can be factory-configured for LVTTL or LVDS operation.

FEATURES:

- 4 AC-Coupled Analog Inputs
- Fs ≤ 160 MHz per channel or Fs ≤ 180 MHz per channel
- Xilinx Virtex-5 SX95T User Programmable FPGA
- PCI-X 64-bit/133 MHz Master/Target Burst Mode DMA capable
- 64 User I/Os via Pn4 connector routed directly to FPGA
- Pn4 LVDS or LVTTL signal levels
- Programmable internal clock
- VxWorks®, Linux® and Windows® software drivers
- Available in extended temperature variants

Independent operation of the two 1 MB FIFOs facilitates simultaneous wideband and narrowband signal processing.

The ICS-1555 can be used with any type of carrier card that will accept a PMC module, including VME, PCI and CompactPCI. When used with an appropriate DSP/processor carrier card, the ICS-1555 offers a powerful single slot solution for software radio applications.

Software development kits are available for VxWorks, Linux and Windows operating systems. Each SDK includes operating examples in 'C'. The Windows SDK also includes a LabVIEW application.

The product is ideally suited for demanding applications in military communications, 3G and 4G cellular base station development, signal intelligence, smart antenna, radar beam forming, wireless test & measurement and satellite ground stations.

abaco SYSTEMS

ICS-1555 *4-Channel, 160/180 MHz 16-bit ADC PMC Module with Virtex-5 SX95T User Programmable FPGA*

Specifications

Analog Input

- Four AC-coupled analog inputs
- 50 ohm input impedance
- Full scale input voltage 1.48 dBm (0.75 Vpp) or 5 dBm (1.125 Vpp), software selectable
- Input signal bandwidth of 2 MHz to 300 MHz (-3 dB point)
- Maximum sample rate of 160 MHz/channel or 180 MHz/channel
- Minimum sample rate of 1 MHz/channel
- Internal sample clock oscillator 100 MHz
- Analog to digital resolution 16-bits
- Sampling on rising edge of internal or external sample clock
- External trigger LVTTL/LVCMOS 5V tolerance, software selectable Rising/ Falling edge
- External sync. LVTTL/LVCMOS 5 V tolerance, software selectable Rising/ Falling edge
- External clock reference LVTTL/Sinewave compatible,-3 dB min. ~ +6 dBm max.
- S/(N+D) > 73 dBFs @ f in = 70 MHz @ 160 MSPS, typ.
- S/(N+D) > 70 dBFs @ f in 90 MHz @ 180 MSPS, typ.
- SFDR 84 dBc @ f in = 70 MHz, typ.

General

- IEEE std. 1386.1-2001 PMC compatible
- VxWorks, Linux and Windows software drivers

Onboard Resources

- Xilinx Virtex-5 SX95T user programmable FPGA
- 2 MBytes of FIFO memory
- SMA connectors

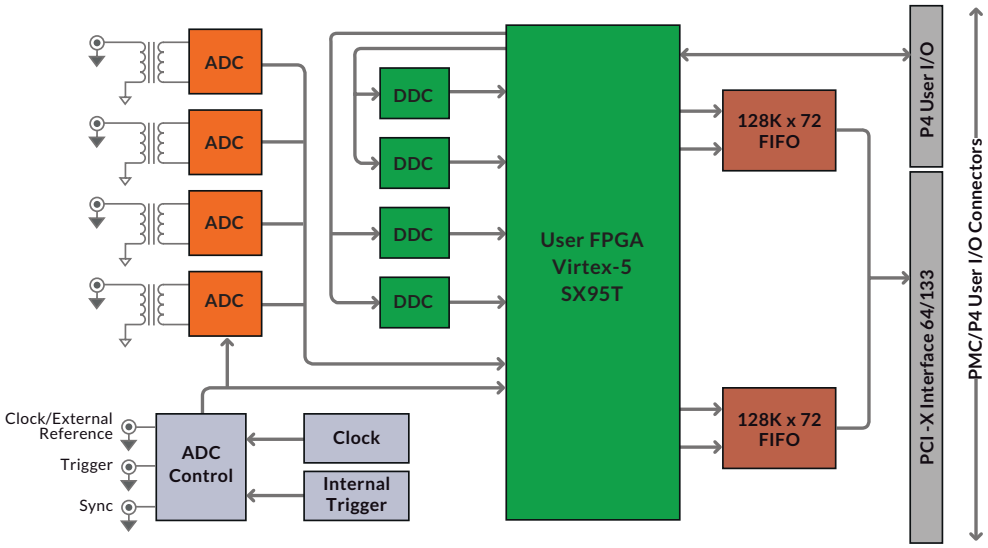
I/O Specifications

- PCI-X 64-bit 133 MHz Master/Target Burst Mode DMA capable
- All 64 user programmable I/O via Pn4 connector router directly to FPGA
- Pn4 user definable LVDS or LVTTL signal levels

Environmental

- Three air-cooled build levels available
- Operating temperature, -40°C to +75°C
- 95% non-condensing humidity
- Required cooling 200 LFM

Block diagram



Ordering information

ICS-1555A-x00	ICS-1555, 160 MHz, 1-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x01	ICS-1555, 160 MHz, 2-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x02	ICS-1555, 160 MHz, 4-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x03	ICS-1555, 160 MHz, 1-channel, with DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x04	ICS-1555, 160 MHz, 2-channel, with DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x05	ICS-1555, 160 MHz, 4-channel, with DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x12	ICS-1555, 180 MHz, 1-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x13	ICS-1555, 180 MHz, 2-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x14	ICS-1555, 180 MHz, 4-channel, no DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x15	ICS-1555, 180 MHz, 1-channel, with DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x16	ICS-1555, 180 MHz, 2-channel, with DDCs, x = ruggedization level 0, 2 or 3
ICS-1555A-x17	ICS-1555, 180 MHz, 4-channel, with DDCs, x = ruggedization level 0, 2 or 3
DRV-1555-VXW	Software development kit for VxWorks operating system
DRV-1555-LX	Software development kit for Linux operating system
DRV-1555-WIN	Software development kit for Windows operating system
HDK-1555	Hardware development kit for FPGA development by user, including a default core (included with board)

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