



SPR870A

3U VPX Wideband Digital Receiver/Exciter Module

The SPR870A builds on the legacy of our industry-leading digital receiver families to bring a new transceiver to market with Xilinx Virtex-6 FPGA technology. Designed for wideband signal acquisition and conversion applications such as radar ECM (digital RF memory) and RF test applications, it provides unsurpassed converter technology with industry-leading FPGA resources. The result is an ultra-high performance wideband digital transceiver in a single 3U VPX slot.

The SPR870A provides a dual channel 10-bit ADC and one 12-bit DAC sampling synchronously at 1.375 GHz. The ADC input pass band is 10 MHz to 2.8 GHz (3dB) to allow for second Nyquist applications.

An open source Xilinx Virtex-6 FPGA is provided for user-defined signal processing functions, giving greater capacity than previous generations. A second Virtex-6 provides a PCIe interface to the system controller. Other protocols, such as sRIO can be provided on request.

The FPGA provides a powerful signal processing capability that can be loaded with standard functions such as wideband DDC, FFT and time stamping, or programmed by the user for any required function.

The product provides internal and external clock and trigger capability. A low speed (250 MHz) ADC input port is provided to accept baseband signals such as log video.

Software Development Kits (SDKs) are available for VxWorks, Linux and Windows operating systems. Each SDK includes operating examples in 'C'.

The Hardware Development Kit (HDK) provides support for users who wish to implement their own signal processing algorithms in the FPGA. Alternatively, our FPGA applications programming team can develop FPGA cores specific to customer needs.

The VPX P2 connector provides direct access to the user FPGA for single ended (LVTTTL) and high speed serial signals. These connections provide alternative high-speed data path to the module via Aurora, PCI Express, or other protocols.

Memory resources consist of four banks of DDR3 SDRAM. Each bank is comprised of three 1Gbit (64MB x 16) SDRAMs configured as a single 48 bit x 64M bank. All are attached to the FPGA for general purpose storage with very high IO bandwidth. The factory installed FPGA core implements a pair of dual bank swing buffers (one for the wideband ADCs, the other for the DACs) but using the HDK, the memory may be reconfigured as the application requires.

The SPR870A can be used in any 3U VPX system that provides PCI Express connectivity on the data plane. When used with an appropriate VPX system controller or single board computer, the SPR870A offers a powerful single slot wideband transceiver solution for radar and software radio applications.

The product is ideally suited for demanding radar applications such as pulse intercept and analysis, electronic countermeasures, and RF test.

FEATURES:

- 2 Transformer-coupled Analog Inputs, 10 bits, $F_s=1.375$ GHz per channel
- 1 Transformer-coupled Analog Outputs, 12 bits, $F_s=1.375$ GHz per channel
- Xilinx Virtex-6 SX475T User Programmable FPGA
- PCIe x4 Master/Target Burst Mode DMA capable
- VxWorks, Linux and Windows software drivers

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Specifications

Analog Input

- One analog inputs, 10-bit, $F_s=1.375$, transformer-coupled, SMA connectors
- SNR > 51 dBFs
- SFDR > 65 dBFs.
- 50 Ohm input/output impedance
- Full scale input voltage 1.8 dBm (0.79 Vpp)
- Input signal bandwidth of 10 MHz to 2.8 GHz (-3 dB point) in 2 channel mode
- Minimum input sample rate of 100 MHz/channel

Analog Output

- One analog outputs, 12-bit, 1.375GHz, transformer-coupled, SMA connectors (2nd DAC optional)
- SFDR > 62dBc
- Full scale output 4 dBm into 50 Ohm load

Clock/Trigger

- Programmable VCXO with 1 Hz resolution & stable 10MHz reference onboard
- Accepts external clock at the sample rate, or at a lower reference frequency (ie; 10MHz).
- Clock input power range -6 dB min. ~ +10 dBm max.
- Log video input allows trigger based on received signal strength.

General

- VITA 46.4 compatible
- VxWorks, Linux and Windows software drivers

Onboard Resources

- Xilinx Virtex-6 SX475T user programmable FPGA
- Four banks of DDR3 SDRAM (64M x 48)
- SMA connectors for I/O

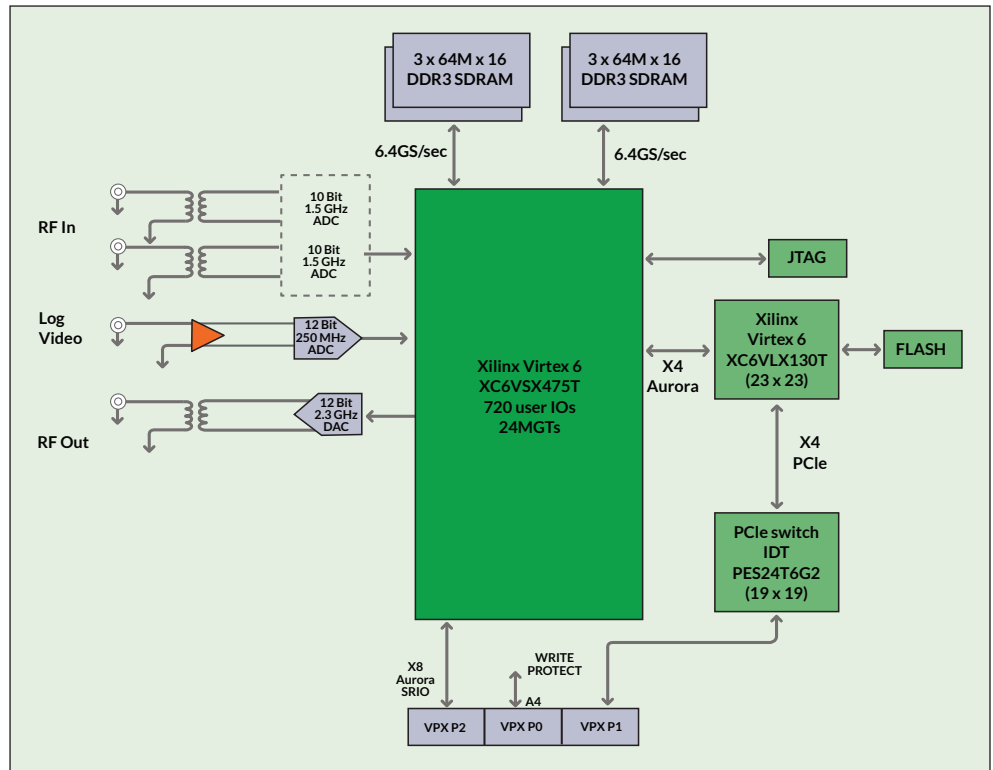
I/O Specifications

- PCIe control plane fabric (VPX P1 data plane)
- 8-lane user-defined GMT/Aurora interface (VPX P2)

Environmental

- Operating temperature -40°C to +85°C
- 95% non-condensing humidity

Block diagram



Ordering information

SPR870A-x00	2-ch ADC, 1-ch DAC, 1-ch Log Video ADC, Four Banks of DDR3 SDRAM, 1.5GB total Virtex-6 SX475T, level 1-4
SWIN-SPR870A-OYSC	Windows Software Development Kit for SPR870A
SLIN-SPR870A-OYSC	Linux Software Development Kit for SPR870A
SVXW-SPR870A-OYSC	VxWorks Software Development Kit for SPR870A

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